AN13942

基于 **i.MXRT595** 的 **Memory-in-Pixel LCD** 驱动应用

Rev. 2 — **2023**年**10**月**16**日 应用笔记

文档信息

信息	内容
关键词	AN13942, i.MXRT595, FlexIO, SmartDMA, Memory-in-Pixel (MiP)
摘要	Memory-in-Pixel (MiP) LCD 专为可穿戴设备和其他小屏幕应用而设计，具有超低功耗常亮显示特点。

1 简介

Memory-in-Pixel (MiP) LCD 专为可穿戴设备和其他小屏幕应用而设计，具有超低功耗常亮显示特点。

i.MX RT595 有两个内置外设，分别是 FlexIO 和 SMARTDMA。FlexIO 是一个可灵活配置的模块，提供广泛的功能。SMARTDMA 是一种图形加速器，用于内存和显示接口之间数据传输。

本文介绍了一种采用 SMARTDMA 和 FlexIO 来驱动 MiP LCD 的应用。用户可以通过设置 FlexIO 和 SMARTDMA 参数来适应新的 MiP LCD 屏。

2 Memory-in-Pixel (MiP) LCD

本章节主要介绍 Memory-in-Pixel (MiP) LCD。

2.1 概述

MiP LCD 非常适合可穿戴和手持产品。 面板的每个像素都有一个 SRAM，可以在没有连续信号输入的情况下存储图像。 在这种情况下，控制器可以处于睡眠模式或完全关闭以实现超低功耗。主要特点如下：

- 反射模式
- 通过 6 位并行的数据信号通讯实现显示控制
- 每个像素是 RGB222 格式，可实现 64 色显示
- 显示面板自带 SDRAM 用于数据存储
- 显示面板具有薄、轻、紧凑特点
- 属于超低功耗的TFT屏

注：在接下来的章节中，将描述和比较两类 MiP LCD 屏。 一个是 JDI 公司生产的，另一个是日本 Sharp 公司生产的。

2.2 输入管脚

MiP 屏输入端子名称和功能如 表 1 所示，左边是 JDI 生产的 LCD 引脚说明，右边是 Sharp 生产的 LCD 说明。两者的控制引脚名称不同，但功能相同，数据引脚名称功能完全相同。

表 1. JDI LCD 和 Sharp LCD 输入管脚对比

JDI's MiP LCD		SHARP's MiP LCD	
PIN	**Description**	**PIN**	**Description**
XRST	Reset signal for the horizontal and vertical driver	INTB	Initial signal for Binary/Gate-Driver
VST	Start signal for the vertical driver	GSP	Start signal for the Gate-Driver
VCK	Shift clock for the vertical driver	GCK	Clock for the Gate-Driver
ENB	Write enable signal for the pixel memory	GEN	Gate Enable Signal
HST	Start signal for the horizontal driver	BSP	Start signal for the Binary-Driver
HCK	Shift clock for the horizontal driver	BCK	Clock for the Bianary-Driver

表 1. JDI LCD 和 Sharp LCD 输入管脚对比...续上页

JDI's MiP LCD		SHARP's MiP LCD	
R[0]	Red image data (odd pixels)	R[0]	Red image data (odd pixels)
R[1]	Red image data (even pixels)	R[1]	Red image data (even pixels)
G[0]	Green image data (odd pixels)	G[0]	Green image data (odd pixels)
G[1]	Green image data (even pixels)	G[1]	Green image data (even pixels)
B[0]	Blue image data (odd pixels)	B[0]	Blue image data (odd pixels)
B[1]	Blueimage data (even pixels)	B[1]	Blue image data (even pixels)
FRP	Liquid crystal driving signal ("Off" pixel)	VB	Black signal voltage of LCD Inphase signal to VCOM
XFRP	Liquid crystal driving signal ("On" pixel)	VA	White signal voltage of LCD oppsite to VCOM
VCOM	Common electrode driving signal	VCOM	Common terminal for LCD/ duty=50 % Square wave

2.3 垂直时序

图 1 显示了两个 MiP LCD 的垂直时序。左边是 JDI 屏时序框图，右边是 Sharp 屏时序框图。其中，彩色椭圆标记出了一些差异：

- VST 信号在 VCK 信号之前触发，但 GSP 信号在 GCK 信号之后触发。
- 每帧的尾部 VCK 信号边沿数与 GCK 信号边沿数不同。
- XRST信号为低电平时有 2 个 VCK 边沿数，而 INTB 为低电平时 GCK 信号边沿数为零。
- ENB 信号在 VCK 信号的第 3 个边沿之后切换，而 GEN 在 GCK 的第 3 个边沿之前切换。

此外，关于延时信息差异需要参考时序约束表，所有差异点都需要是可配置的。

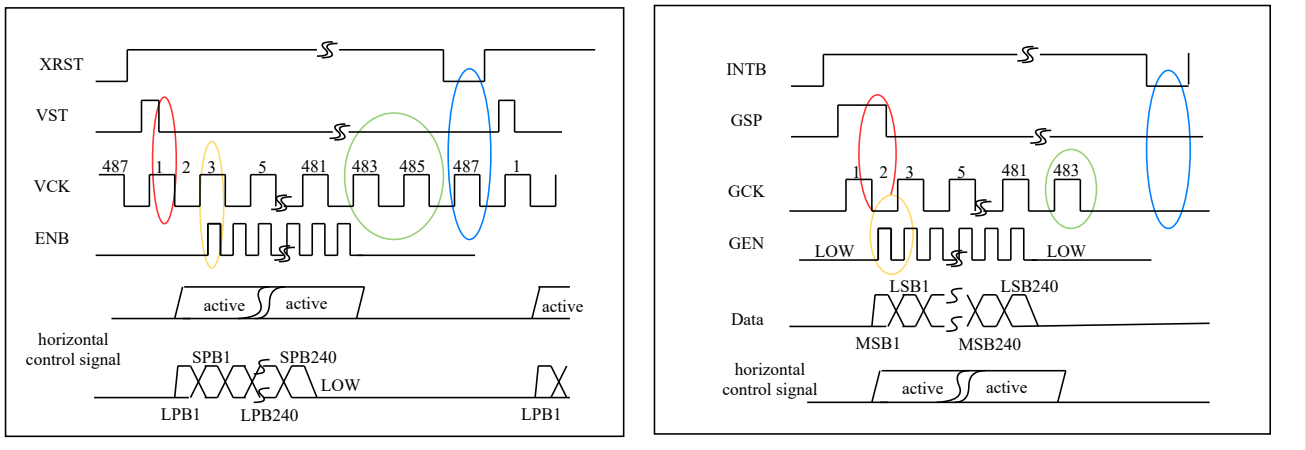

图 1. 垂直时序比较

2.4 水平时序

图 2 显示了两个 MiP LCD 的水平时序。左边为 JDI 屏时序框图，右边是 Sharp 屏时序框图。

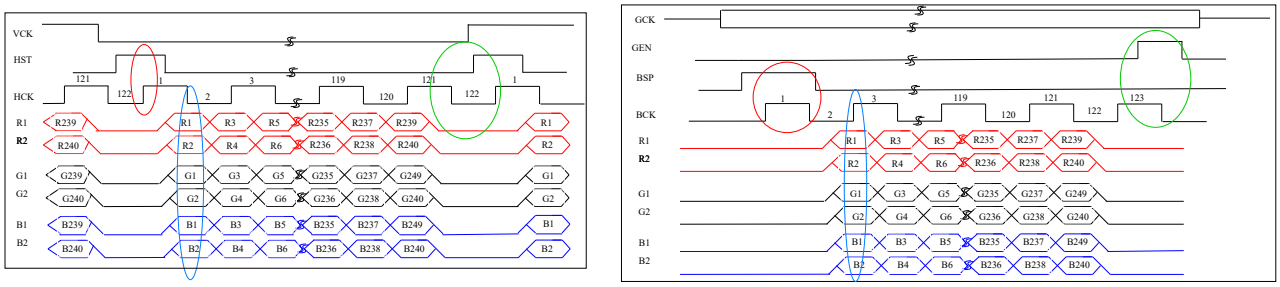

图 2. 水平时序比较

部分差异点如下所示：

- HCK 信号边沿数与 BCK 边沿边沿数不同。
- HST 信号高电平时，HCK 信号只有一个边沿，BSP 信号高电平时，BCK 信号有两个边沿。
- RGB 数据在 HCK 信号的第 2 个边沿发送，但在 BCK 信号的第 3 个边沿发送。
- 其他一些与时序条件相关的差异。

2.5 部分更新模式时序

以 JDI 的 LPM012M387D 屏为例，图 3 显示了屏在部分更新模式下的时序。当更新 80 - 160 行图像时，时序图如 图 3。

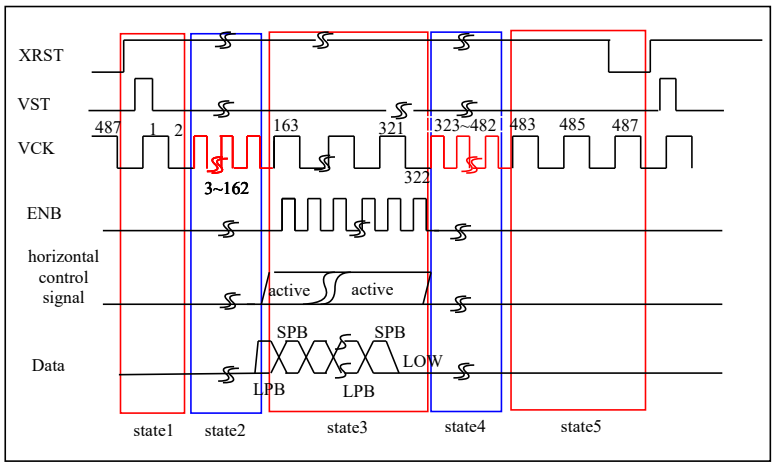

图 3. 部分更新模式的五个状态

如 图 3 所示，时序可以分为五种状态：

- 状态一：XRST信号由低电平切换到高电平，为每一帧的起始状态。
- 状态二：非更新状态（从 0 行到 79 行)，只有快速 VCK 信号。
- 状态三：更新状态（从 80 行到 160 行），其中有标准 VCK 信号。
- 状态四：非更新状态（从 161 行到 239 行），和状态二相同。
- 状态五：每一帧的结束状态。

当更新整行图像时，时序图只有三个状态：状态一、状态三和状态五。Sharp 的 MiP LCD 也有类似的五种状态。

3 MiP 并行接口实现

3.1 硬件概述

硬件链接如 图 4 所示。

由 SMARTDMA 控制的输出管脚如下：

- P4_20：为 VST 或 GSP 信号线。
- P4_21：为 FlexIO 时钟, 输出到管脚 P5_1。
- P4_22：为 XRST 或 INITB 信号线。
- P4_23：为 VCK 或 GCK 信号线。

由 FlexIO 控制的输出管脚如下：

- P4_24 - P4_29：RGB 数据信号线，Shifter0 每个移位时钟输出 8 比特数据，其中低 6 位输出控制位RGB数据。
- P4_30：为 ENB 或 GEN 信号线，由 shifter0 的 BIT6 控制。
- P4_31：为 HST 或 BSP 信号，由 shifter0 的 BIT6 控制。
- P5_0：为 HCK 或 BCK 提供时钟，由定时器控制。

FlexIO的输入管脚：

- P5_1：P4_21 输出被接到 P5_1，为 shifter 提供时钟，为定时器提供 trigger 信号。

VCOM 时钟管脚：

- P5_2 & P5_3：为 VCOM/FRP/XFRP(VCOM/VA/VB) 提供时钟。

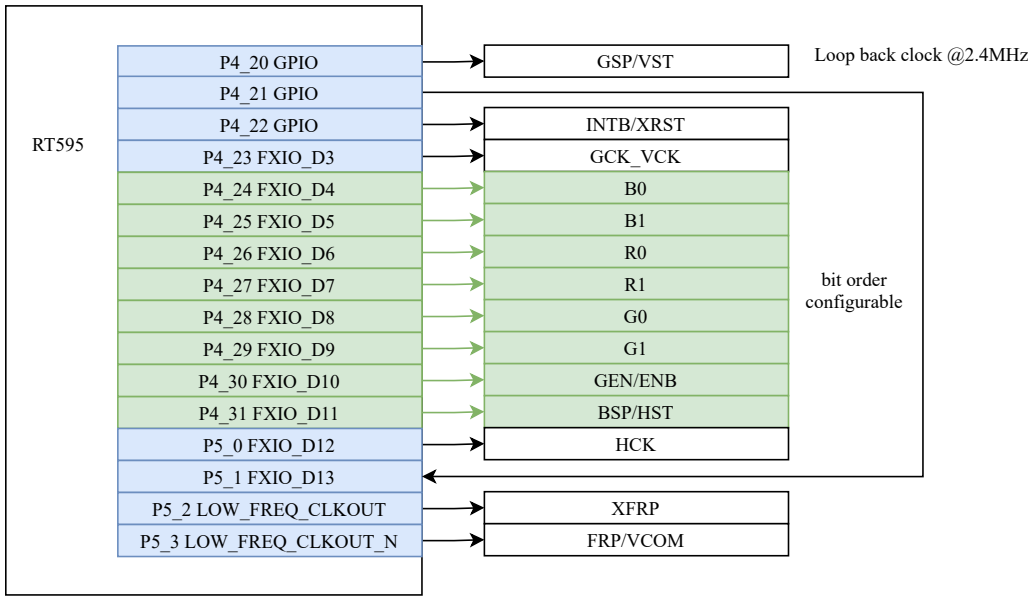

图 4. 硬件连接图

3.2 FlexIO 配置

如 图 5 所示，结合 GPIO，FlexIO 用了 2 个移位器，3 个定时器来实现 MiP 并行时序。

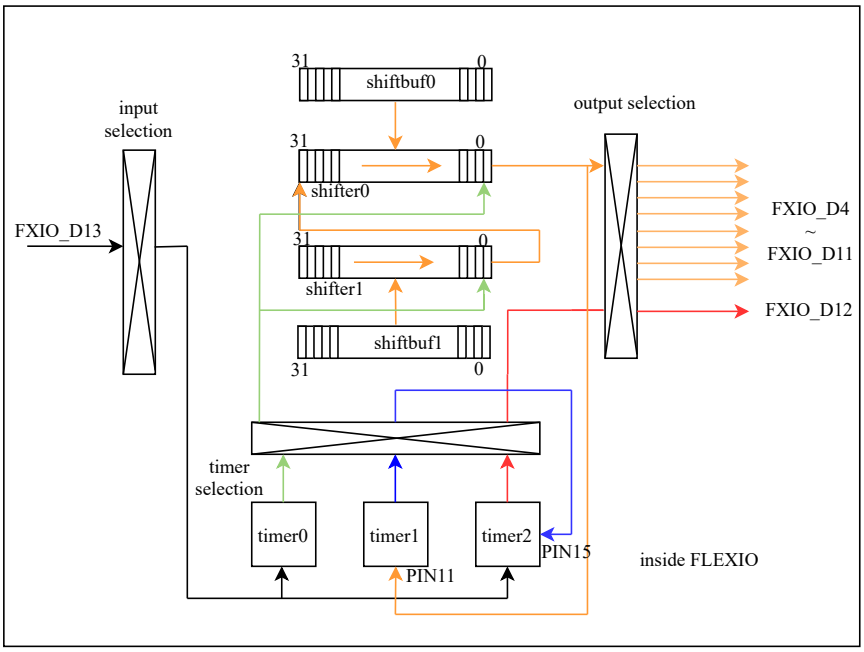

图 5. FlexIO 内部连接

表 2 描述了用于连接 64 色 MiP LCD 模块的 FlexIO 配置。

表 2. MiP LCD 接口配置

计数器	取值	说明
SHIFTCFG0/1	0x0007_0100	配置移相器的输入来自相邻移相器输出，8 比特宽数据。
SHIFTCTL0	0x0003_0402	数据发送到 FXIO_D4 - D11 管脚，在使用定时器 0 输出信号的上升沿发数。
SHIFTCTL1	0x0000_0002	上升沿传数。
TIMCTL0	0x1A40_0003	16 位计数模式，使用 FXIO_D13 作为计时触发信号。
TIMCFG0	0x0170_0000	初始输出为低电平，减计数，移位时钟等于输入触发信号频率。
TIMCMP0	0x0007	16 位计数模式。
TIMCTL1	0x1643_0F81	配置双 8 位计数器波特率模式，内部触发，FXIO_D11 为触发引脚，FXIO_D15为输出引脚。
TIMCFG1	0x0000_2600	单程计数器。
TIMCMP1	0x0113	双 8 位宽计数值。
TIMCTL2	0x1E43_0C41	双 8 位计数器，内部触发信号 D15 作为触发信号，输入时钟从 D13 管脚来，输出时钟到 D12 管脚。
TIMCFG2	0x0220_2600	减计数。
TIMCMP2	0x7901	双 8 位计数器，高 8 位为时钟数，低 8 位为周期数。

3.3 MiP 引擎配置

MiP LCD 驱动在此文档又被称为“MiP引擎”，MiP 引擎数据结构定义了一套参数集，这些参数用于控制 MiP 引擎的行为。数据结构的具体定义如 参数结构 所示：

参数结构

```
typedef struct _mip_engine _config
{
    uint32_t s1DelayXrstVst; /* delay from reset signal to vertical start signal
 in state1, unit: /5us*/
    uint32_t s1DelayVstVck; /* delay from vertical start signal to vertical
 clock signal in state1, unit: /5us */
    uint32_t s1TwVstH;  /* vst high-level width  in in state1, unit: /5us */
    uint32_t s1TwVckH; /* vck high-level width in state1, unit: /5us */
    uint32_t s2TwFastVckH; /* high width of fast vck, uint: 20ns */
    uint32_t s3DelayShiftClock; /*delay to toggle the first flexio clock(shift
 clock) */
    uint32_t s3DelayHstHck; /* delay from horizontal start signal to the first
 horizontal clock, in state3 */
    uint32_t s3HckNum; /* the number of the hck edge, in state3 */
    uint32_t s3TwHckH; /* 1/2 cycle of hck, in state3 */
    uint32_t s5VckNum; /* num of VCK edge in state 5 */
    uint32_t s5ExtraVckNum; /* number of vck between two frames in state5 */
}
mip_engine_config_t;
typedef struct _smartdma_mip_display_config
{
    uint32_t *pdmaStart; /* the start address of data buffer */
    uint32_t startline; /* the first line to be updated, index starts with zero
 */
    uint32_t endline; /* the last line to be updated, index starts with */
    uint32_t panelWidth; /* panel width, equal to resolution */
    uint32_t panelHeight; /* panel height, equal to resolution*/
    uint32_t dataWidth; /* the number of bytes each line, should be a multiple
 of 4 bytes*/
    uint32_t freq; /* 0: 99Mhz, 1:198Mhz */
    mip_engine_config_t *pEnginePara; /* pointer to the paras for MIP engine
 mip_engine_config_t */
    uint32_t *smartdmaStack; /* the stack defined by software */
}
smartdma_mip_display_config_t;
```

smartdma_mip_display_config_t 结构体中的绝大多数参数和头文件 fsl_mip_engine_config.h 中的宏值一一映射，可以通过修改宏值来直接修改参数的值。头文件中的宏如 fsl_mip_engine_config.h 头文件 所示：

fsl_mip_engine_config.h 头文件

```
/*! @brief the width of the LCD panel */
#define DISPLAY_PANEL_WIDTH 240
/*! @brief the height of the LCD panel */
#define DISPLAY_PANEL_HEIGHT 240
/*! @brief the byte number of data for each line, 4-byte address-aligned
*/
#define DISPLAY_DATA_WIDTH ((((DISPLAY_PANEL_WIDTH >> 1) + 2) + 3) & (~0x3))
/*! @brief the number of lines, each line includes lsb line and msb line */
#define DISPLAY_DATA_HEIGHT ((DISPLAY_PANEL_HEIGHT << 1) + 2)
/*! @brief the delay time from toggling the xrst signal
* to toggling the vst signal, unit is 5.05 us
```

```
*/
#define DISPLAY_DELAY_XRST_VST (3)
/*! @brief the delay time from toggling the vst signal
* to toggling the vck signal, unit is 5.05 us
*/
#define DISPLAY_DELAY_VST_VCK (6)
/*! @brief the hold time of VST, unit is 5.05us */
#define DISPLAY_TWVSTH (6)
/*! @brief the high-level width of VCK, uint is 5.05us */
#define DISPLAY_TWVCKH (13)
/*! @brief the high-level width of fast VCK, unit is 20ns */
#define DISPLAY_FAST_VCK_WIDTH (50)
/*! @brief the delay time to toggle the first flexio clock, unit is 20ns */
#define DISPLAY_DELAY_SHIFT_CLK (20)
/*! @brief the delay time from toggling the hst signal
* to toggling the hck signal,
* used to configure timer1 of flexio, timer1 is used to triggle time2
*/
#define DISPLAY_DELAY_HST_HCK (FLEXIO_TIMCMP_CMP((2-1)<<8 | (20-1)<<0))
/*! @brief the number of hck, each line, used to configure timer2 of flexio */
#define DISPLAY_HCK_NUM (((DISPLAY_PANEL_WIDTH >> 1) + 2 - 1))
/*! @brief the low or high width of hck, used to configure timer2 of flexio */
#define DISPLAY_HCK_WIDTH (2-1)
/*! @brief the number of vck after finishing data sending, in state5 */
#define DISPLAY_S5_VCKNUM (4)
/*! @brief the extra number of vck in state5 */
#define DISPLAY_S5_EXTRA_VCK_NUM (2)
```

接下来的章节是关于参数的说明。

3.3.1 状态一参数

这部分参数控制着状态一的时序。四个参数分别是 s1DelayXrstVst, s1DelayVstVck, s1TwVstH and s1TwVckH，如 图 6 所示:

- s1DelayXrstVst：XRST 信号上升沿到 VST 信号上升沿延时，单位 5 us。
- s1DelayVstVck：VST 信号上升沿到 VCK 信号上升沿延时，单位 5 us。
- s1TwVstH：VST 信号高电平维持时间，单位 5 us。
- s1TwVckH：VCK 信号高电平维持时间，单位 5 us。

用户可以调整这个四个参数的值来满足不同屏幕的状态一时序要求。

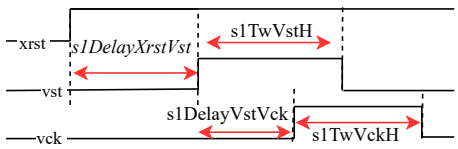

图 6. 状态一控制参数

以 LPM012M387D 模块为例，为满足其状态一时序要求，参数设置如 状态一参数值 所示：

状态一参数值

```
s1DelayXrstVst =3; /* tsXRST=15 us, > 12.8us, DISPLAY_DELAY_XRST_VST used
 instead */
s1DelayVstVck =6; /* tsVST=30us, > 24 us */
s1TwVstH =6; /* thVST=30us, >24.8us */
```

```
s1TwVckH =13; /* 65us, > 48us */
```

3.3.2 状态二参数

状态二下并不更新像素信息，只刷新 VCK 信号用于切换行。当从 LCD 屏幕中间位置刷新图像时候，需要输出一些快速 VCK 时钟。如 图 7 所示：

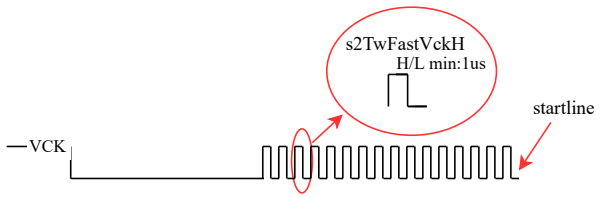

图 7. 状态二的高速 **VCK** 信号

状态二的 VCK 数量和周期受如下两个参数控制：

- startLine：定义 FastVCK 沿数量。
- s2TwFastVckH：高电平维持时间，定义 FastVck 周期（单位 20 ns，占空比 50 %）。

以 LPM012M387D 模块为例，当从 80 行开始刷新时候，为满足其状态二时序要求，参数设置如 状态二参数值 所示：

状态二参数值

```
startLine=80; /* the start line index is just 80 */
s2TwFastVck=50; /* 50 * 20 ns=1us, DISPLAY_FAST_VCK_WIDTH is used instead*/
```

3.3.3 状态三参数

该状态是正常刷新图像的状态，所有的控制信号和数据信号都要被控制。

- 垂直控制信号：包括触发时间，VCK 周期和边沿数。
- 水平控制信号：HST 信号触发时间和高电平宽度，HCK 触发时间、周期长度和边沿数。
- 写使能信号：ENB 信号触发时间和高电平宽度。
- 数据信号：包括 R0，R1，G0，G1，B0，B1。

这部分参数使用稍微复杂些，具体说明如下所述：

- 对于 VCK 信号：
  - s3DelayShiftClock：定义触发第一个移位时钟（FlexIO clock）的延时，单位 20 ns。
  - dataWidth：定义高电平时间，同时控制着 FlexIO clock 时钟数。

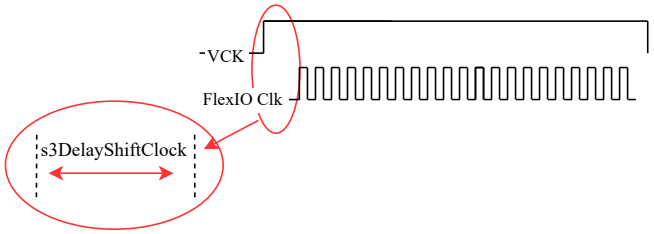

图 8. **VCK** 宽度和 **FlexIO clock** 触发开始延时

  - startLine, endLine：控制着 VCK 信号开始和结束，也就是状态三 VCK 边沿数。

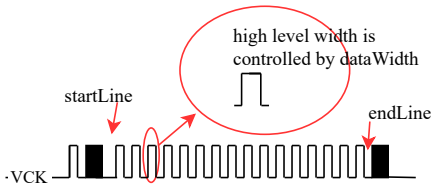

图 9. VCK 边沿数和周期

- 对于 HST 和 ENB 信号：
  这两个信号和 RGB 数据一起构成数据信号。用户可以通过修改 fill_buffer_HST_ENB(uint32_t startline, uint32_t endline) 函数的实现来控制这两个信号，包括 HST 的触发时间和高电平维持时间，以及 ENB 触发时间和高电平维持时间。

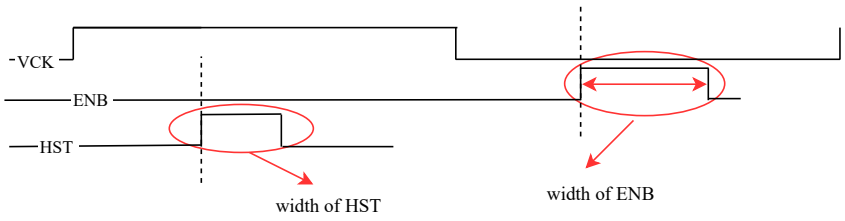

图 10. HST 和 ENB 信号

- 对于 HCK 信号：
  - s3DelayHstHck：定义 HST 信号上升沿到 HCK 第一个上升沿的延时，值等于宏定义 DISPLAY_DELAY_HST_HCK。
  - s3HckNum：定义 VCK 信号高电平或低电平期间的 HCK 边沿数，值等于宏定义 DISPLAY_HCK_NUM。
  - s3TwHckH：定义 HCK 信号高电平维持时间，值等于宏定义 DISPLAY_HCK_WIDTH。

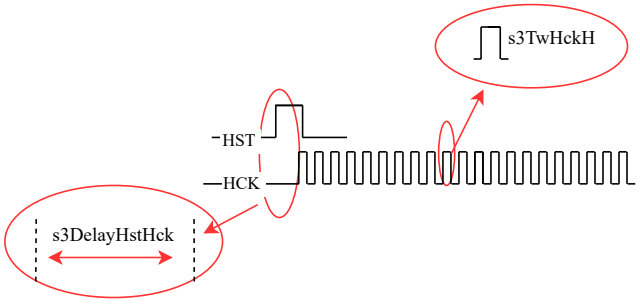

图 11. HCK 相关参数

- 对于数据信号，具体值由用户自己定义。
  以 LPM012M387D 模块为例，当刷新第 80 到 160 行像素时，具体参数设置如 状态三参数 所示。

状态三参数

```
startLine = 80; /* update from line 80 */
endLine = 160; /* update to line 160 */
freq = 1; /* reflect the frequency for SmartDMA*/
dataWidth = 124; /* */
s3DelayHstHck = DISPLAY_DELAY_HST_HCK#
s3HckNum = DISPLAY_HCK_NUM#
s3TwHckH = DISPLAY_HCK_WIDTH#
```

3.3.4 状态四参数

状态四和状态二相同，当刷新部分行时候，如果刷新结束行不是面板的最后一行，MiP 引擎需要输出一些快速 VCK 时钟，如 图 12 所示。状态四相关参数：

- endLine：控制状态四 VCK 起始位置。
- lastLine：控制 VCK 结束位置。

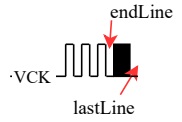

图 12. 状态四参数

以 LPM012M387D 模块为例，当部分刷新第 80 到 160 行像素时，参数设置如 状态四参数 所示：

状态四参数

```
endLine=160; /* just equal to the value in state three */
lastLine=239; /* its resolution is 240x240, so is (240-1)*/
```

3.3.5 状态五参数

状态五为一帧图像时序的结束状态。如 图 13 所示，不同 LCD 的 VCK 信号边沿数不同。

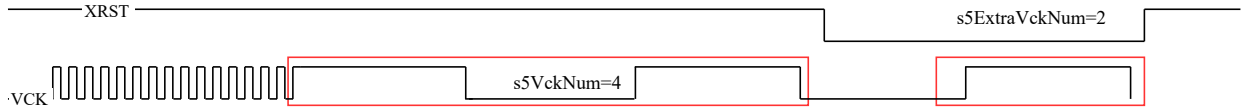

图 13. 状态五参数

在该状态下，有两个相关参数

- s5VckNum：控制状态五有多少个 VCK 边沿。
- s5ExtraVckNum：控制状态五是否有额外的 VCK 边沿。

以 LPM012M387D 模块为例，具体参数设置如 状态五参数值 所示：

状态五参数值

```
s5VckNum = 4; /* 4 edges of vck after state 4*/
s5ExtraVckNum = 2; /* a vck exist between two frame */
```

3.4 仿真结果概述

以 LPM012M387D 模块为例，当刷新 80 到 160 行时，逻辑分析仪捕获的部分信号时序图，如 图 14 所示。

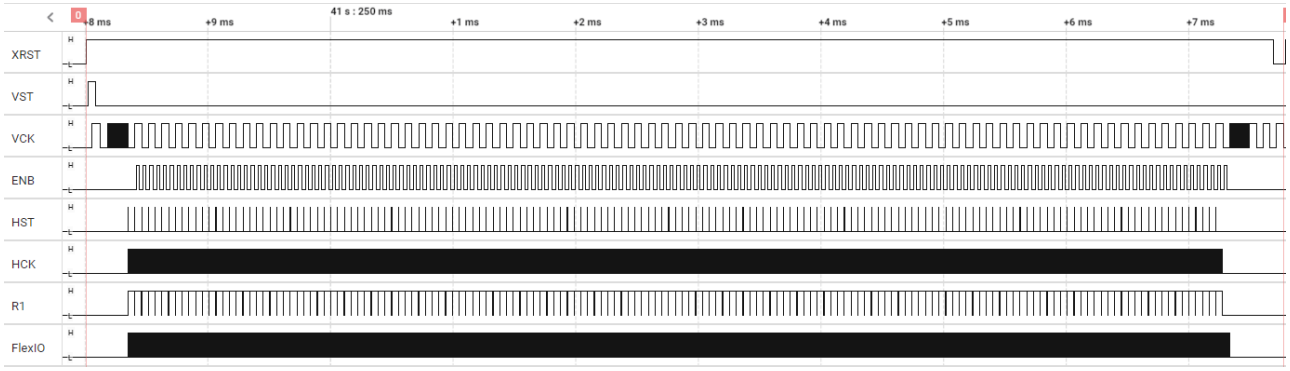

图 **14.** 部分刷新模式

4 结论

这篇应用笔记描述了如何使用 FlexIO 和 SMARTDMA 来模拟 MiP 并行接口，并对引擎相关参数做出详细解释，该引擎可以支持大部分并行的 64 色的 MiP LCD 面板。目前支持如下：

- JDI 生产的 64 色并行 MiP LCD 屏
- Sharp 生产的 64 色并行 MiP LCD 屏

5 参考文献

1. i.MX RT500 Low-Power Crossover MCU Reference Manual (文档 iMXRT500RM)
2. Using FlexIO for Parallel Camera Interface (文档 AN5275)
3. Using FlexIO to Drive 8080 Bus Interface LCD Module (文档 AN5313)
4. The specification of LPM012M387D
5. The specification of LS012B7DD06

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7 修订记录

表 3 汇总了自初始版以来对本文档所做的更改。

修订记录

版本号	日期	说明
2	2023 年 10 月 16 日	图片更新成 svg 格式
1	2023 年 6 月 21 日	初次发布

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基于 **i.MXRT595** 的 **Memory-in-Pixel LCD** 驱动应用

内容

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